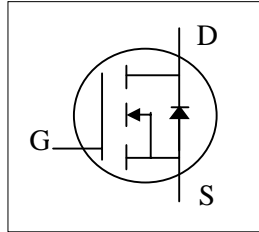




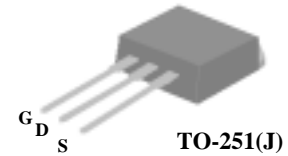
- ▼ Low on-resistance
- ▼ Capable of 2.5V gate drive
- ▼ Low drive current
- ▼ Single Drive Requirement



$BV_{DSS}$	20V
$R_{DS(ON)}$	50m $\Omega$
$I_D$	20A

**Description**

The Advanced Power MOSFETs from APEC provide the designer with the best combination of fast switching, ruggedized device design, ultra low on-resistance and cost-effectiveness.



**Absolute Maximum Ratings**

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	20	V
$V_{GS}$	Gate-Source Voltage	$\pm 12$	V
$I_D@T_C=25^\circ C$	Continuous Drain Current, $V_{GS}$ @ 4.5V	20	A
$I_D@T_C=125^\circ C$	Continuous Drain Current, $V_{GS}$ @ 4.5V	16	A
$I_{DM}$	Pulsed Drain Current <sup>1</sup>	41	A
$P_D@T_C=25^\circ C$	Total Power Dissipation	26	W
	Linear Derating Factor	0.2	W/ $^\circ C$
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ C$

**Thermal Data**

Symbol	Parameter	Value	Unit
Rthj-c	Thermal Resistance Junction-case	Max. 4.8	$^\circ C/W$
Rthj-a	Thermal Resistance Junction-ambient	Max. 110	$^\circ C/W$



**Electrical Characteristics @T<sub>j</sub>=25°C(unless otherwise specified)**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	20	-	-	V
ΔBV <sub>DSS</sub> /ΔT <sub>j</sub>	Breakdown Voltage Temperature Coefficient	Reference to 25°C, I <sub>D</sub> =1mA	-	0.03	-	V/°C
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =4.5V, I <sub>D</sub> =6A	-	-	50	mΩ
		V <sub>GS</sub> =2.5V, I <sub>D</sub> =5.2A	-	-	80	mΩ
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA	0.5	-	1.2	V
g <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> =10V, I <sub>D</sub> =6A	-	13	-	S
I <sub>DSS</sub>	Drain-Source Leakage Current (T <sub>j</sub> =25°C)	V <sub>DS</sub> =20V, V <sub>GS</sub> =0V	-	-	1	uA
	Drain-Source Leakage Current (T <sub>j</sub> =125°C)	V <sub>DS</sub> =16V, V <sub>GS</sub> =0V	-	-	25	uA
I <sub>GSS</sub>	Gate-Source Leakage	V <sub>GS</sub> = ± 12V	-	-	±100	nA
Q <sub>g</sub>	Total Gate Charge <sup>2</sup>	I <sub>D</sub> =10A	-	7.5	-	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>DS</sub> =20V	-	0.9	-	nC
Q <sub>gd</sub>	Gate-Drain ("Miller") Charge	V <sub>GS</sub> =5V	-	4	-	nC
t <sub>d(on)</sub>	Turn-on Delay Time <sup>2</sup>	V <sub>DS</sub> =10V	-	4.5	-	ns
t <sub>r</sub>	Rise Time	I <sub>D</sub> =10A	-	49.5	-	ns
t <sub>d(off)</sub>	Turn-off Delay Time	R <sub>G</sub> =3.3Ω, V <sub>GS</sub> =5V	-	12	-	ns
t <sub>f</sub>	Fall Time	R <sub>D</sub> =1Ω	-	6	-	ns
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V	-	195	-	pF
C <sub>oss</sub>	Output Capacitance	V <sub>DS</sub> =20V	-	126	-	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	f=1.0MHz	-	50	-	pF

**Source-Drain Diode**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I <sub>S</sub>	Continuous Source Current ( Body Diode )	V <sub>D</sub> =V <sub>G</sub> =0V , V <sub>S</sub> =1.3V	-	-	20	A
I <sub>SM</sub>	Pulsed Source Current ( Body Diode ) <sup>1</sup>		-	-	41	A
V <sub>SD</sub>	Forward On Voltage <sup>2</sup>	T <sub>j</sub> =25°C, I <sub>S</sub> =20A, V <sub>GS</sub> =0V	-	-	1.3	V

**Notes:**

- 1.Pulse width limited by safe operating area.
- 2.Pulse width ≤300us , duty cycle ≤2%.

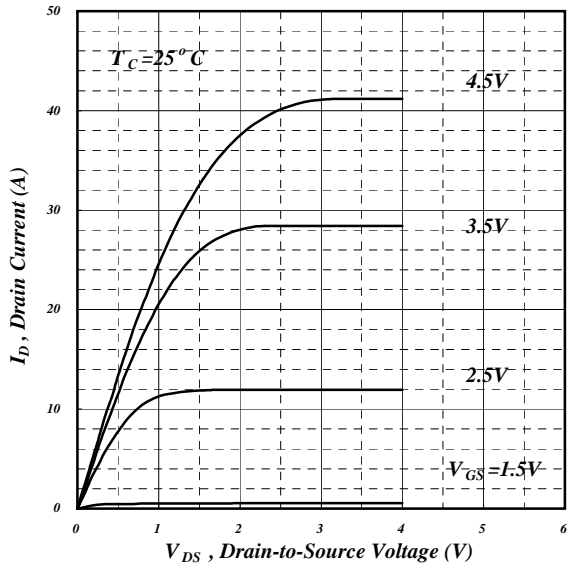


Fig 1. Typical Output Characteristics

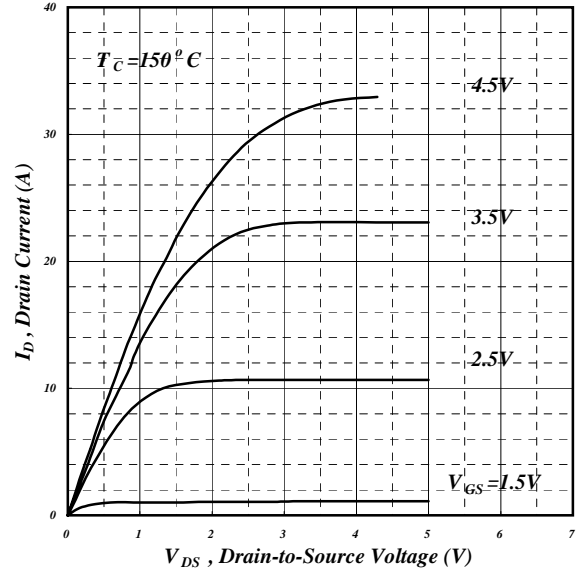


Fig 2. Typical Output Characteristics

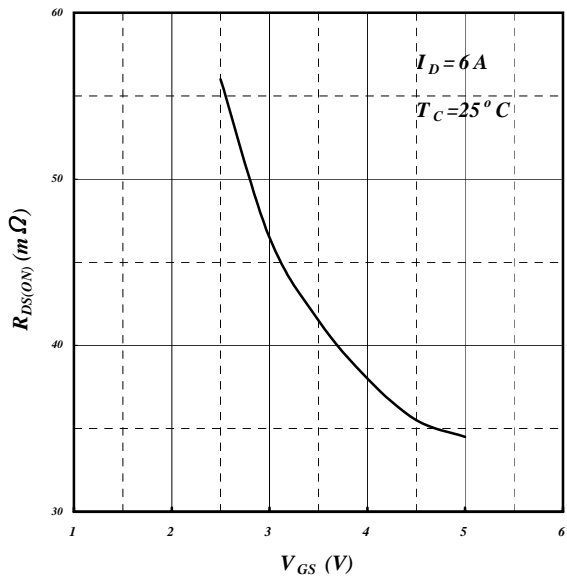


Fig 3. On-Resistance v.s. Gate Voltage

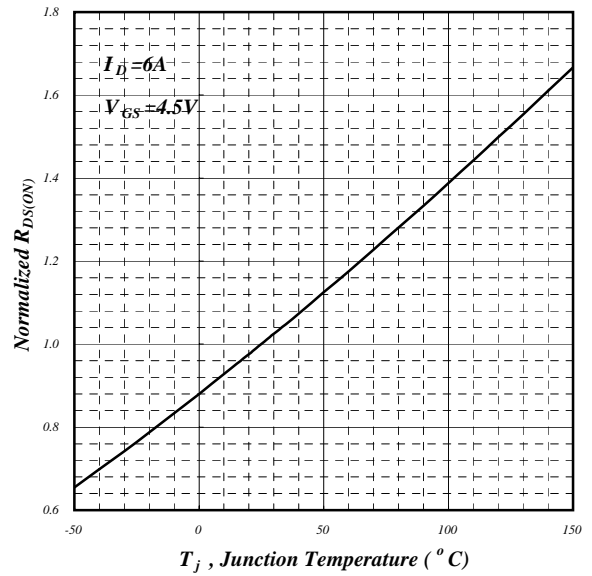


Fig 4. Normalized On-Resistance v.s. Junction Temperature

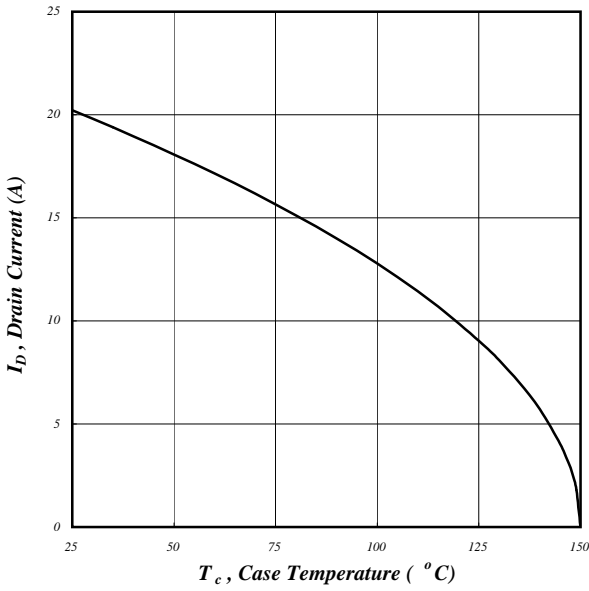


Fig 5. Maximum Drain Current v.s. Case Temperature

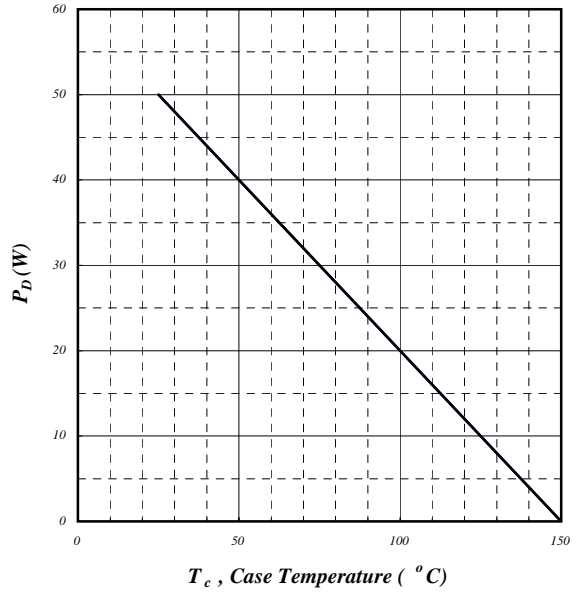


Fig 6. Typical Power Dissipation

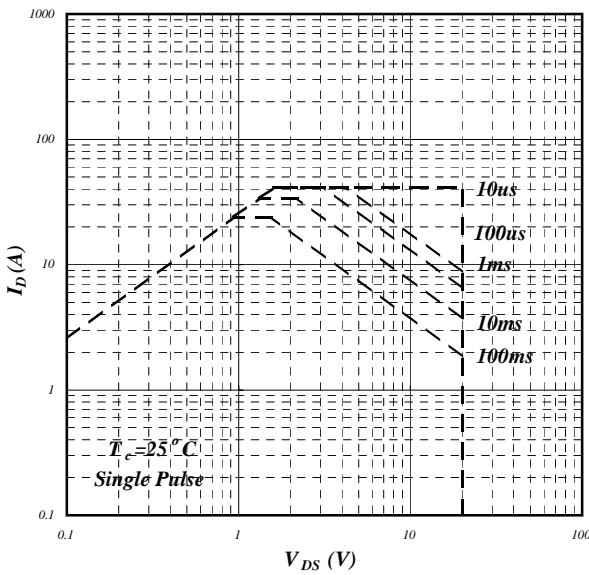


Fig 7. Maximum Safe Operating Area

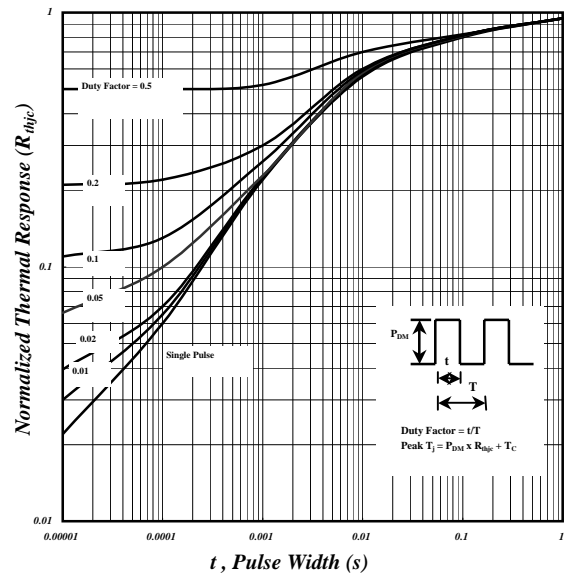


Fig 8. Effective Transient Thermal Impedance

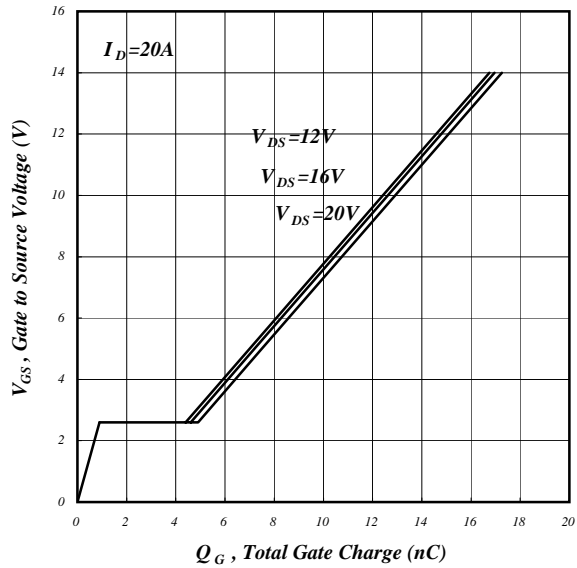


Fig 9. Gate Charge Characteristics

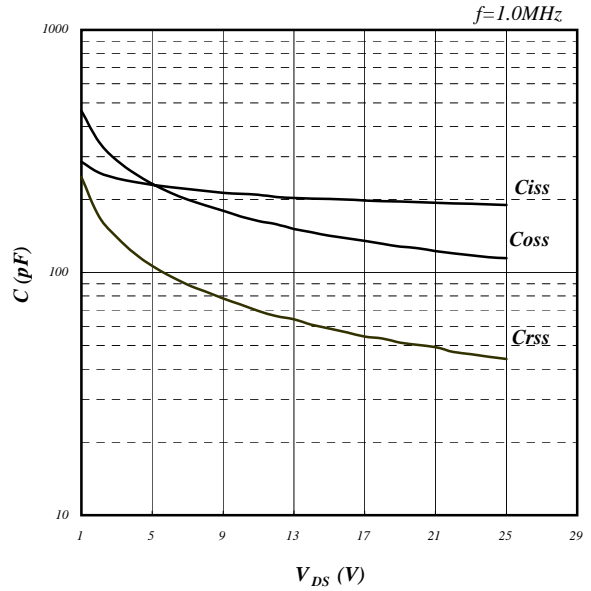


Fig 10. Typical Capacitance Characteristics

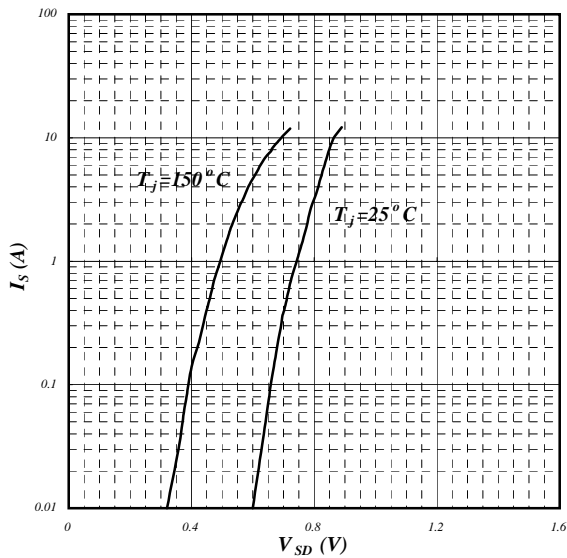


Fig 11. Forward Characteristic of Reverse Diode

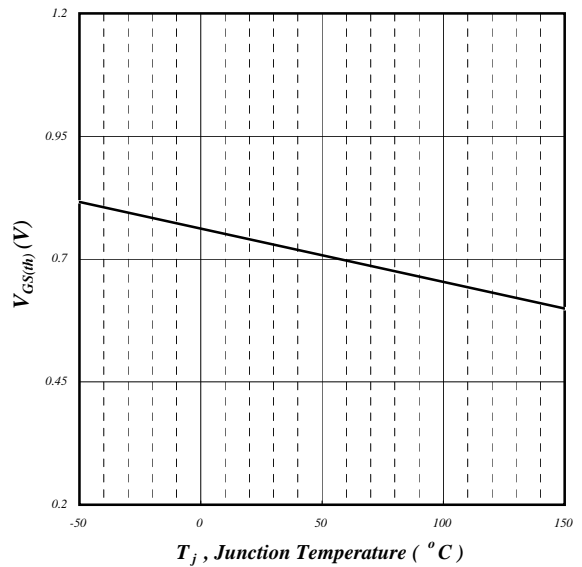


Fig 12. Gate Threshold Voltage v.s. Junction Temperature

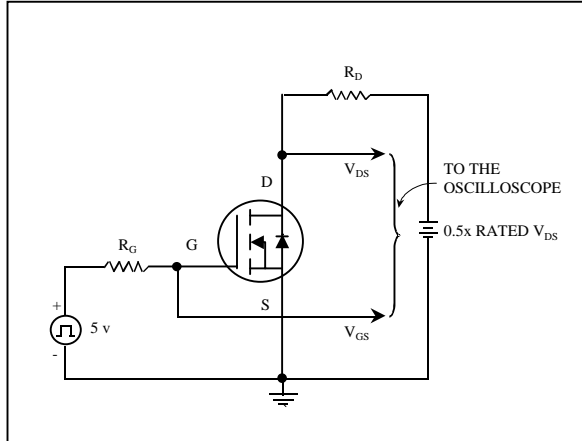


Fig 13. Switching Time Circuit

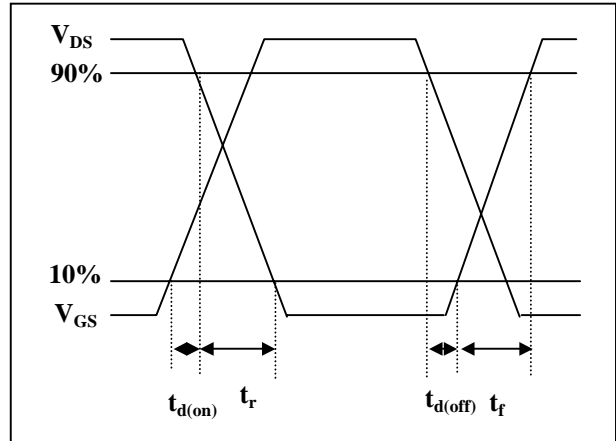


Fig 14. Switching Time Waveform

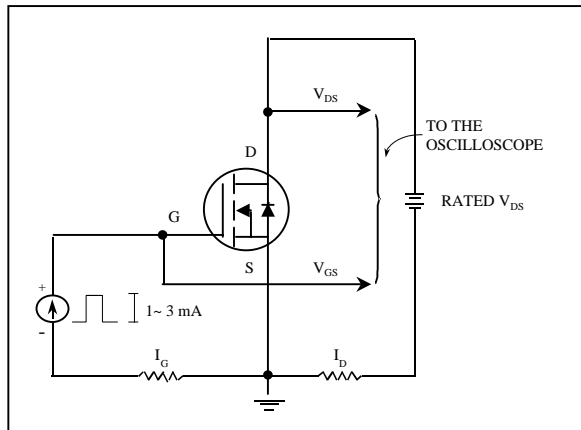


Fig 15. Gate Charge Circuit

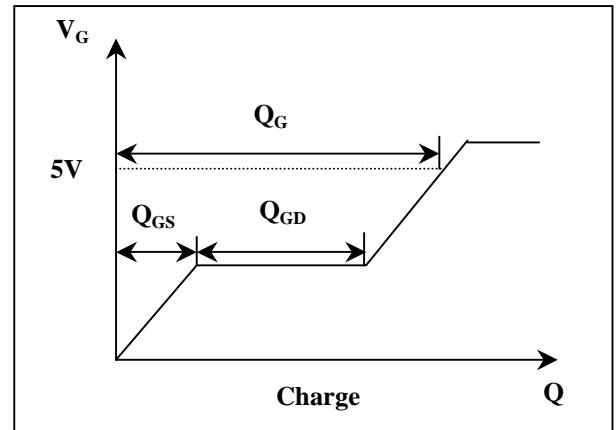


Fig 16. Gate Charge Waveform